CPRE 4920 Status Report 03

2/26/2025 – 03/12/2026

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Cache Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

  Since the last status update, we have finished the core design and made major progress on the core controller design. We have also started the integration of all of our top-level components.

- **Past Week Accomplishments**

  - Colin McGann: Added user data to rasterizer and worked on normal calculation. Also worked on core integration
  - Jack Tonn: Finished core implementation and made good progress on the documentation of the cores. I also looked into the chipfoundry competition, which could give us a free tapeout
  - Dawud Benedict: Working through cache synthesis
  - Michael Drobot: Added commercial SRAM BRAM wrapper, core controller bugfixes and testing. Out sick for most of week 2.
  - Sam Forde: Cleaned up and finished rewriting spi memory chip model. Wrote documentation for implementing the commercial SRAM.
  - Josh Arceo: Finished mailman/fragment fifo design and testing, added some more modules to optimization table before running out of storage

- Emil Kosic: Finished HDL for wb to pk bridge and majority of basic testing.

- **Pending Issues**
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- **Individual contributions**

NAME	Individual Contributions	Hours this period	HOURS cumulative
Colin McGann	Integrated top level, fixed texture scaling for rasterizer	40	350
Jack Tonn	Fixed da core issues, did documentation	40	280
Dawud Benedict	Cache synth, sram synth	25	163
Michael Drobot	Core controller bug fixes	20	342
Sam Forde	Cleaned up SPI chip model, wrote documentation	23	136
Josh Arceo	Finished Fragment fifo, optimized modules	25	130
Emil Kosic	Wb to pk bridge rtl and testing	25	146

- **Plans for the upcoming weeks**
  - Colin McGann: Will finish normal calcs and continue integration once others are done with their modules
  - Jack Tonn: Finish core documentation and submit uGPU to the design competition
  - Dawud Benedict: Synth Cache and finally start something with the last required stuff.
  - Michael Drobot: Integrate core controller with cores and rasterizer.
  - Sam Forde: Write more documentation, assist with implementing SRAM into other designs, pick up slack elsewhere
  - Josh Arceo: Complete optimization table, assist in documentation
  - Emil Kosic: Add more in-depth tests to catch all cases for the bridge and synthesize